-- 19. The processor of Claim 15, wherein the processor generates said output bit stream at said output as a function of one or more Boolean operations performed on said input bit streams.--

-- 20. The processor of Claim 15, wherein each said input combination of said plurality of input combinations at said one or more inputs is operated on by said opcode.--

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-- 21. The processor of Claim 15, wherein each of said one or more inputs accommodates a single serial bit stream.--

-- 22. The processor of Claim 15, wherein said opcode is defined by a predetermined set of Boolean operations.--

-- 23. The processor of Claim 22, wherein said opcode is generated from a lookup table having a finite number of said input combinations mapped to a respective single bit result, said single bit result obtained in accordance with said set of predetermined Boolean operations.--

-- 24. The processor of Claim 23, wherein each said respective single bit result of said finite number of said input combinations is used to generate a string of said single bit results which define said opcode.--

-- 25. A method for bit stream processing, comprising the steps of:

providing a memory having one or more inputs for receiving respective input bit streams, the input bit streams of the one or more inputs defining a plurality of input combinations to the memory;

inputting a selected one of one or more opcodes at an opcode input of the memory, which the selected one of the one or more opcodes operates on the input combinations; and

outputting an output bit stream at an output of the memory.--

-- 26. The method of Claim 25, wherein the memory in the step of providing is a bit-addressable memory where each input combination of the plurality of input combinations is mapped to a unique bit location in the memory.--

-- 27. The method of Claim 25, wherein the memory in the step of providing comprises binary memory devices which can be individually and selectively read.--

-- 28. The method of Claim 25, wherein the plurality of input combinations in the step of providing comprise separate address inputs which are selected by the select one of the one or more opcodes.--

-- 29. The method of Claim 25, wherein the processor in the step of outputting generates the output bit stream at the output as a function of one or more Boolean operations performed on the input bit streams.--

-- 30. The method of Claim 25, wherein each input combination of the plurality of input combinations at the one or more inputs is operated on individually by the opcode, in the step of inputting.--

-- 31. The method of Claim 25, wherein each of the one or more inputs in the step of providing accommodates a single serial bit stream.--

-- 32. The method of Claim 25, wherein the opcode in the step of inputting is defined by a predetermined set of Boolean operations.--

-- 33. The method of Claim 32, wherein the opcode is generated from a lookup table having a finite number of the input combinations mapped to a respective single bit result, the single bit result obtained in accordance with the set of predetermined Boolean operations.--